Customer No.: 31561
Docket No.: 12258-US-PA
Application No.: 10/708,522

REMARKS

Present Status of the Application

The Office Action has rejected claims 1-6 under 35 U.S.C. 112, first paragraph, because the specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with the claims. To satisfy this enablement requirement, Applicant is required to clarify the issues which have not yet been satisfactorily resolved and consequently raise doubt as to enablement.

Discussion of claim rejections under 35 USC 112

Claims 1-6 have been rejected under 35 U.S.C. 112, first paragraph, because the specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with the claims.

Applicant respectfully submits that the rejection under 35 U.S.C. 112, first paragraph, is improper, and thus should be withdrawn.

In detail, referring to the specification, the present invention is directed to a dither algorithm including a plurality of frames scanned with a plurality of pixels, and each of the pixels includes a plurality of bits. An observed unit is defined as a 4x2 block of the pixels and has a first sub unit and a second sub unit. Each of the sub units has a 2x2 block of the pixels. For each of the pixels of the first sub unit and of the second sub unit, the

dither algorithms are demonstrated in FIGs. 3A and 3B, respectively. As illustrated in FIGs. 3A and 3B, the input patterns (the 2-bit LSBs) are defined to be at 00, 10, 01 or 11, 01, and 11. Five different settings of the 2-bit LSBs result in 6 different operations in repeated sequential fashion.

The descriptions regarding the pixel of the first sub unit of the observed unit are taken as a factual support of the claimed subject matter. In the amended specification, it is clearly explained that when the 2-bit LSBs are at 00, no operation is rendered. When the 2-bit LSBs are at 01, a first operation is rendered in repeated sequential fashion in a four-frame period to an upper-left pixel, a lower-right pixel, a lower-left pixel, and an upper-right pixel. When the 2-bit LSBs are at 10, a second operation is rendered in repeated sequential fashion in a two-frame period to the pixels of the lower row and the pixels of the upper row. When the 2-bit LSBs are at 11, a third operation is rendered as the first operation is. When the 2-bit LSBs are at 01 or 11, the moving pixel (being carry for 01 case; being not carry for 11 case) goes upper-left, lower-right, lower-left, and upper-right sequentially in the first 2x2 block, and goes lower-left, and upper-right, upper-left, lower-right sequentially in the next 2x2 block, thus makes a 4x2 block.

Further, the paragraph [0013] of the present invention is interpreted in another systematic and accessible way as follows: a dither algorithm including a plurality of frames scanned with a plurality of pixels is provided. Each of the pixels includes a plurality of bits. An observed unit is defined as a 4x2 block of the pixels and has a first sub unit and a second sub unit. Each of the sub units has a 2x2 block of the pixels. For

each of the pixels of the first sub unit of the observed unit, the dither algorithm includes the following operations. When 2-bit LSBs are at 00, no operation is rendered. When the 2-bit LSBs are at 01, a first operation is rendered in repeated sequential fashion in a four-frame period to an upper-left pixel, a lower-right pixel, a lower-left pixel, and an upper-right pixel. When the 2-bit LSBs are at 10, a second operation is rendered in repeated sequential fashion in a two-frame period to the pixels of the lower row and the pixels of the upper row. Here, the moving pixel always moves up and down. The average value of 2 on the screen is provided, and no drawback as described is found. When the 2-bit LSBs are at 11, a third operation is rendered as the first operation is. That is to say, when the 2-bit LSBs being 01 or 11, the moving pixel (being carry for 01 case; being not carry for 11 case) goes upper-left, lower-right, lower-left, and upper-right sequentially in the first 2x2 block, and goes lower-left, and upper-right, upper-left, lower-right sequentially in the next 2x2 block, thus makes a 4x2 block. On the other hand, for each of the pixels of the second sub unit of the observed unit, the dither algorithm further includes the following operations. When the 2-bit LSBs are at 00, no operation is rendered. When the 2-bit LSBs are at 01, a fourth operation is rendered in repeated sequential fashion in the four-frame period to the lower-left pixel, the upper-right pixel, the upper-left pixel, and the lower-right pixel. When the 2-bit LSBs are at 10, a fifth operation is rendered in repeated sequential fashion in the two-frame period as the second operation is. When the 2-bit LSBs are at 11, a sixth operation is rendered in a repeated sequential fashion in the four-frame period as the fourth operation is.

Furthermore, the paragraph [0014] of the present invention is interpreted in another

systematic and accessible way as follows: another dither algorithm is similar to the foregoing method, yet the moving rule of the carry element is reverse to the preceding one. In the dither algorithm, a plurality of frames scanned with a plurality of pixels is provided. Each of the pixels includes a plurality of bits. An observed unit is defined as a 4x2 block of the pixels and has a first sub unit and a second sub unit. Each of the sub units has a 2x2 block of the pixels. For each of the pixels of the first sub unit of the observed unit, the dither algorithm includes the following operations. When a 2-bit LSBs are at 00, no operation is rendered. When the 2-bit LSBs are at 01, a first operation is rendered in repeated sequential fashion in a four-frame period to an upper-left pixel, an upper-right pixel, a lower-left pixel, and a lower-right pixel. When the 2-bit LSBs are at 10, a second operation is rendered in repeated sequential fashion in a two-frame period to the lower row and the upper row. Here, the moving pixel always moves up and down, being the same as the first embodiment described above. The average value of 2 on the screen is provided accordingly. When the 2-bit LSBs are at 11, a third operation is rendered as the first operation is. That is to say, when the 2-bit LSBs being 01 or 11, the moving pixel (being carry for 01 case; being not carry for 11 case) goes upper-left, upper-right, lower-left, and lower-right sequentially in the first 2x2 block, and goes lower-left, lower-right, upper-left, and upper-right sequentially in the next 2x2 block, thus makes a 4x2 block. On the other hand, for each of the pixels of the second sub unit of the observed unit, the dither algorithm includes the following operations. When the 2-bit LSBs are at 00, no operation is rendered. When the 2-bit LSBs are at 01, a fourth operation is rendered in repeated sequential fashion in the four-frame period to the lower-left pixel,

the lower-right pixel, the upper-left pixel, and the upper-right pixel. When the 2-bit LSBs are at 10, a fifth operation is rendered as the second operation is. When the 2-bit LSBs are at 11, a sixth operation is rendered as the fourth operation is. In this moving fashion, an average value of 1 or 3 on the screen is observed. Because there is no horizontal line staying at the same position every two frames, the moving pixels or lines on the screen is not observed on the screen. Besides, the basic observed unit of the invention is the 4x2 block and the adjacent 2x2 blocks behave differently, so dithered edges are not performed. Therefore, 3D dither problems are solved according to this another preferred embodiment of the present invention.

Accordingly, it is submitted that the invention is able to be communicated to the interested public in a meaningful way. Since the information contained in the disclosure of the application is deemed sufficient to inform those skilled in the relevant art how to both make and use the claimed invention, claims 1 and 4 should be definite, well supported by the Applicant's disclosure, and patentable.

Likewise, claims 2-3 and 5-6 respectively depending on allowable independent claims 1 and 4 are now placed in proper condition for allowance under the same rationale as a matter of law.

Customer No.: 31561
Docket No.: 12258-US-PA
Application No.: 10/708,522

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-6 are in proper condition for allowance and an action to such effect is earnestly solicited. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date : August 30, 2007

Belinda Lee

Belinda Lee
Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw